ANNA UNIVERSITY OF TECHNOLOGY MADURAI
MADURAI -625002

REGULATIONS 2010

CURRICULUM & SYLLABI

M.E. VLSI DESIGN

SEMESTER I

<table>
<thead>
<tr>
<th>S No.</th>
<th>Subject Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Theory</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>10277AM101</td>
<td>Applied Mathematics</td>
<td>3</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>10244VL102</td>
<td>Nano CMOS Device Architecture</td>
<td>3</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>10244AE103</td>
<td>Advanced Digital System Design</td>
<td>3</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>10244VL104</td>
<td>VLSI Design Techniques</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>10244VL105</td>
<td>Solid State Device Modeling and Simulation</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>E01</td>
<td>Elective I</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Practical</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>10244VL107</td>
<td>VLSI Design Laboratory I</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>2</td>
</tr>
</tbody>
</table>

Total 23

SEMESTER II

<table>
<thead>
<tr>
<th>S No.</th>
<th>Subject Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Theory</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>10244AE201</td>
<td>Analysis and Design of Analog Integrated Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>10244VL202</td>
<td>VLSI Device and Process Simulation</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>10244VL203</td>
<td>Computer Aided Design of VLSI Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>10244AE204</td>
<td>Embedded Systems</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>E02</td>
<td>Elective II</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>E03</td>
<td>Elective III</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Practical</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>10244VL207</td>
<td>VLSI Design Laboratory II</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>2</td>
</tr>
</tbody>
</table>

Total 20
### SEMESTER III

<table>
<thead>
<tr>
<th>S No.</th>
<th>Subject Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>E04</td>
<td>Elective IV</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>E05</td>
<td>Elective V</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>E06</td>
<td>Elective VI</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>

#### Practical

<table>
<thead>
<tr>
<th>S No.</th>
<th>Subject Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>10244VL301</td>
<td>Project Work Phase I</td>
<td>0</td>
<td>0</td>
<td>12</td>
<td>6</td>
</tr>
</tbody>
</table>

**Total** 15

### SEMESTER IV

<table>
<thead>
<tr>
<th>S No.</th>
<th>Subject Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10244VL401</td>
<td>Project Work Phase II</td>
<td>0</td>
<td>0</td>
<td>24</td>
<td>12</td>
</tr>
</tbody>
</table>

**Total** 12

Total Credits to be Earned for the Award of the Degree = 70
### LIST OF ELECTIVES

<table>
<thead>
<tr>
<th>S No.</th>
<th>Subject Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ELECTIVE I (E01)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>10244VLE11</td>
<td>ASIC Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>10244AE105</td>
<td>Advanced Microprocessors and Microcontrollers</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>10244VLE13</td>
<td>Digital Signal Processing of Integrated Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td><strong>ELECTIVE II (E02)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>10244VLE21</td>
<td>Analog VLSI Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>10244VLE22</td>
<td>Testing of VLSI Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td><strong>ELECTIVE III (E03)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>10244VLE31</td>
<td>Design of semiconductor Memories</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>7</td>
<td>10244VLE32</td>
<td>VLSI Technology</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td><strong>ELECTIVE IV (E04)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>10244VLE41</td>
<td>Physical Design of VLSI Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>9</td>
<td>10244VLE42</td>
<td>Genetic Algorithms and their Applications</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>10</td>
<td>10244AEE41</td>
<td>Electromagnetic Interference and Compatibility in System Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td><strong>ELECTIVE V (E05)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>10244CCE23</td>
<td>Neural Networks and Applications</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>12</td>
<td>10244VLE51</td>
<td>Low power VLSI Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>13</td>
<td>10244AEE31</td>
<td>Reliability Engineering</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td><strong>ELECTIVE VI (E06)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>10244CME23</td>
<td>Digital Speech Signal Processing</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>15</td>
<td>10244CME22</td>
<td>DSP Processor Architecture and programming</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>16</td>
<td>10244VLE61</td>
<td>VLSI Signal Processing</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>
10277AM101 - APPLIED MATHEMATICS

UNIT I  LINEAR ALGEBRAIC EQUATIONS & EIGEN VALUE PROBLEMS  9

UNIT II  MATRIX THEORY  9

UNIT III  ONE DIMENSIONAL RANDOM VARIABLES  9

UNIT IV  DYNAMIC PROGRAMMING  9

UNIT V  QUEUEING MODELS  9

TEXT BOOKS:

REFERENCES
# NANO CMOS DEVICE ARCHITECTURE

**Unit I**  
**INTRODUCTION**

Physics of Scaling - Device parameters for superior performance - Threshold voltage - Historical trends - International Technology Roadmap for Semiconductors - Different scaling methods - Ballistic transistors

**Unit II**  
**SHORT CHANNEL EFFECTS**

Short channel effects - Threshold voltage roll-off - Drain induced barrier lowering - Punch through - hot carrier degradation - velocity saturation - reverse short channel effects - interconnects

**Unit III**  
**VLSI DEVICES**

Break through solutions - Source/Drain engineering - Channel engineering - Vertical substrate engineering - Halo implants - Gate oxide engineering - high k dielectrics - gate engineering - DMG MOSFETs

**Unit IV**  
**SOI DEVICES**

Silicon on insulator technology - types - advantages over bulk MOSFETs - metal gate technology - double gate MOSFETs - types, vertical DG MOSFETs, Single electron transistor - types, advantages - issues.

**Unit V**  
**EMERGING DEVICES**

Emerging Devices - FINFETS - Surrounding gate - Omega gate MOSFETs - Silicon nanowires - Carbon nano tubes.

L: 45 T: 15 TOTAL: 60

**REFERENCES:**

10244AE103 - ADVANCED DIGITAL SYSTEM DESIGN

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9
Analysis of Asynchronous Sequential Circuit (ASC) - Flow Table Reduction - Races in ASC - State Assignment - Problem and the Transition Table - Design of ASC - Static and Dynamic Hazards - Essential Hazards - Data Synchronizers - Designing Vending Machine Controller - Mixed Operating Mode Asynchronous Circuits.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9
EPROM to Realize a Sequential Circuit - Programmable Logic Devices - Designing a Synchronous Sequential Circuit using a GAL - EPROM - Realization State machine using PLD - FPGA - Xilinx FPGA - Xilinx 2000 - Xilinx 3000- Xilinx 4000

UNIT V SYSTEM DESIGN USING VHDL 9

L: 45 T: 15 TOTAL: 60

TEXT BOOKS:
REFERENCES:
10244VL104  VLSI DESIGN TECHNIQUES

UNIT I  MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY  9
NMOS and PMOS transistors - Threshold voltage - Body effect - Design equations - Second order effects - MOS models and small signal AC characteristics - Basic CMOS technology.

UNIT II  INVERTERS AND LOGIC GATES  9
NMOS and CMOS Inverters - Stick diagram - Inverter ratio - DC and transient characteristics - switching times - Super buffers - Driving large capacitance loads - CMOS logic structures - Transmission gates - Static CMOS design - Dynamic CMOS design.

UNIT III  CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION  9
Resistance estimation - Capacitance estimation - Inductance - Switching characteristics - Transistor sizing - Power dissipation and design margining - Charge sharing - Scaling.

UNIT IV  VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN  9
Multiplexers - Decoders - comparators - Priority encoders - Shift registers - Arithmetic circuits - Ripple carry adders - Carry look ahead adders - High-speed adders - Multipliers- Physical design - Delay modelling - Cross talk - Floor planning - Power distribution - Clock distribution - Basics of CMOS testing.

UNIT V  VERILOG HARDWARE DESCRIPTION LANGUAGE  9
Overview of digital design with Verilog HDL - Hierarchical modelling concepts - Modules and port definitions - Gate level modeling - Data flow modeling - Behavioral modeling - Task & functions - Test Bench.

TOTAL: 45

TEXT BOOKS:

REFERENCES:
UNIT I MOSFET DEVICE PHYSICS
MOSFET capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II NOISE MODELING
Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuits

UNIT III BSIM4 MOSFET MODELING
Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, noise model, junction diode models, Layout-dependent parasitics model.

UNIT IV OTHER MOSFET MODELS
The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, noise model temperature effects, MOS model 9, MOSAI model)

UNIT V MODELLING OF PROCESS VARIATION AND QUALITY ASSURANCE
Influence of process variation, modeling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests

TOTAL: 45

REFERENCES:

10244VL107 VLSI DESIGN LABORATORY I

1. System design using PIC Microcontroller.
2. Implementation of Adaptive Filters- periodogram and multistage multirate system in DSP Processor
3. Analysis of Multirate signals using Simulation Packages
4. Modeling of Sequential Digital system using VHDL.
5. Modeling of Sequential Digital system using Verilog.
6. Design and Implementation of ALU using FPGA.
7. Simulation of NMOS and CMOS circuits using SPICE.
8. System design using 16-bit Microprocessor.

TOTAL: 60
10244AE201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 9

UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC 9
Current sources - Analysis of difference amplifiers with active load using BJT and FET - Supply and temperature independent biasing techniques - Voltage references - Output stages - Emitter follower - Source follower.

UNIT III OPERATIONAL AMPLIFIERS 9
Analysis of operational amplifiers circuit - Slew rate model and high frequency analysis - Frequency response of integrated circuits - Single stage and multistage amplifiers - Operational amplifier noise.

UNIT IV ANALOG MULTIPLIER AND PLL 9
Analysis of four quadrant and variable trans conductance multiplier - Voltage controlled oscillator - Closed loop analysis of PLL - Monolithic PLL design in integrated circuits - Sources of noise - Noise models of Integrated - Circuit Components - Circuit Noise Calculations - Equivalent Input Noise Generators - Noise Bandwidth - Noise Figure and Noise Temperature.

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY 9

TOTAL: 45

TEXT BOOKS:

REFERENCES:
UNIT I  Overview of MOS device scaling and CMOS process flow, Introduction to device and process CAD, Hierarchy of simulation tools, Formulation of device and process equations, Ion implantation.

UNIT II  Equivalent circuit models and carrier Transport equations: DC, Small-Signal, Large Signal models, Boltzmann transport equation, Drift-diffusion approximation, Classical Semiconductor equations, modeling generation and recombination, Thermal characteristics

UNIT III Analytical device models and Hot electron and quantum models: Closed form analytical models of semiconductor devices p-n junction, MOSFET, JFET and MESFETs, HEMTs

UNIT IV  Number solution and Monte carlo simulations: Finite difference method, Finite element method, Monte carlo simulation of semiconductor materials and devices, processing and interpretation of Monte carlo results, Device modeling using Monte Carlo simulations.

UNIT V Hot-electron and quantum models and case simulation studies: Semi classical semiconductor equations, Ballistic transport, Quantum-mechanical effects, One-dimensional, Two dimensional, and Three dimensional simulations

TOTAL: 45

REFERENCES:

UNIT I  VLSI FUNDAMENTALS  

UNIT II  TOPOLOGY RULES AND ALGORITHMS  
Layout Compaction – Design rules – Problem formulation – Algorithms for Constraint Graph Compaction – Placement and partitioning – Circuit representation – Placement algorithms – Partitioning

UNIT III  FLOOR PLANNING AND ROUTING  
Floor Planning concepts – Shape functions and Floorplan sizing – Types of Local Routing problems – Area routing – Channel routing – Global routing – Algorithms for Global Routing

UNIT IV  MODULING AND SIMULATION  
Simulation – Gate–level modeling and simulation – Switch–level modeling and simulation – Combinational Logic Synthesis – Binary Decision Diagrams – Two Level Logic Synthesis

UNIT V  SCHEDULING AND ALGORITHMS  
High level Synthesis – Hardware models – Internal representation – Allocation assignment and scheduling – Simple Scheduling algorithm – Assignment problem – High level transformations

TOTAL: 45

TEXT BOOKS:

REFERENCES:
UNIT I  EMBEDDED ARCHITECTURE  9

UNIT II  EMBEDDED PROCESSOR AND COMPUTING PLATFORM  9

UNIT III  NETWORKS  9

UNIT IV  REAL–TIME CHARACTERISTICS  9

UNIT V  SYSTEM DESIGN TECHNIQUES  9

TOTAL: 45

REFERENCES:
1. System design using PLL.
2. System design using CPLD.
3. Alarm clock using embedded micro controller.
5. Elevator controller using embedded micro controller.
7. Simulation of Adaptive Digital Control System using MAT LAB control system toolbox.

TOTAL: 60
UNIT I
INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance - Logical effort - Library cell design - Library architecture.

UNIT II
PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA - Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III
PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY

UNIT IV
LOGIC SYNTHESIS, SIMULATION AND TESTING
Verilog and logic synthesis - VHDL and logic synthesis - types of simulation - boundary scan test - fault simulation - automatic test pattern generation.

UNIT V
ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING
System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow - global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL: 45

REFERENCES:
UNIT I  MICROPROCESSOR ARCHITECTURE  9

UNIT II  HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM  9

UNIT III  HIGH PERFORMANCE RISC ARCHITECTURE – ARM  9
Organization of CPU – Bus architecture – Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV  MOTOROLA 68HC11 MICROCONTROLLERS  9
Instruction set addressing modes – operating modes- Interrupsysstem- RTC-Serial Communication Interface – A/D Converter PWM and UART.

UNIT V  PIC MICROCONTROLLER  9

TOTAL: 45

REFERENCES:

UNIT I  DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 9

UNIT II  DIGITAL SIGNAL PROCESSING 9

UNIT III  DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

UNIT IV  DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9
DSP system architectures – Standard DSP architecture – Ideal DSP architectures – Multiprocessors and multicomputers – Systolic and Wave front arrays – Shared memory architectures Mapping of DSP algorithms onto hardware – Implementation based on complex PEs – Shared memory architecture with Bit– serial PEs

UNIT V  ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9
Conventional number system – Redundant Number system – Residue Number System Bit–parallel and Bit–Serial arithmetic – Basic shift accumulator – Reducing the memory size – Complex multipliers – Improved shift–accumulator Layout of VLSI circuits – FFT processor – DCT processor and Interpolator as case studies

TOTAL : 45

TEXT BOOKS:
REFERENCES:
UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING 9
Mixed Signal VLSI Chips - Basic CMOS Circuits - Basic Gain Stage - Gain Boosting Techniques -
Super MOS Transistor - Primitive Analog Cells - Linear Voltage - Current Converters - MOS
Multipliers and Resistors - CMOS Op-Amp Design - Instrumentation Amplifier Design - Low
Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT-MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9
Continuous Time Signal Processing - Sampled Data Signal Processing - Switched-Current Data
Converters - Practical Considerations in SI Circuits Biologically-Inspired Neural Networks -
Floating - Gate- Low Power Neural Networks - Networks - Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS 9
First order and Second SC Circuits - Bilinear Transformation - Cascade Design - Switched -
Capacitor Ladder Filter - Synthesis of Switched - Current Filter - Nyquist rate A/D Converters -
Modulators for Over sampled A/D Conversion - First and Second Order and Multibit Sigma - Delta
Modulators - Interpolative Modulators - Cascaded Architecture - Decimation Filters - mechanical -
Thermal - Humidity and Magnetic Sensors - Sensor Interfaces.

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9
Fault modelling and Simulation - Testability - Analysis Technique - Ad Hoc Methods and General
Guidelines - Scan Techniques - Boundary Scan Built-in Self Test - Analog Test Buses - Design for
Electron - Beam Testability - Physics of Interconnects in VLSI Scaling of Interconnects - A Model

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG DIGITAL
LAYOUT 9
Review of Statistical Concepts - Statistical Device Modeling - Statistical Circuit Simulation -
Automation Analog Circuit Design - automatic Analog Layout - CMOS Transistor Layout - Resistor

TOTAL: 45
TEXT BOOKS:

REFERENCES:
UNIT I  BASICS OF TESTING AND FAULT MODELLING  9
Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models –
Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation –
Delay models – Gate Level Event – driven simulation.

UNIT II  TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL 9
CIRCUITS
Test generation for combinational logic circuits – Testable combinational logic circuit design –
Test generation for sequential circuits – design of testable sequential circuits.

UNIT III  DESIGN FOR TESTABILITY 9
Design for Testability – Ad-hoc design – generic scan based design – classical scan based
design – system level DFT approaches.

UNIT IV  SELF – TEST AND TEST ALGORITHMS 9
Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures –
Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V  FAULT DIAGNOSIS 9
Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational
Circuits – Self-checking design – System Level Diagnosis.

TOTAL: 45

REFERENCES:
UNIT I  RANDOM ACCESS MEMORY TECHNOLOGIES  

UNIT II  NONVOLATILE MEMORIES  
Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-GateEPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

UNIT III  MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE  

UNIT IV  RELIABILITY AND RADIATION EFFECTS  

UNIT V  PACKAGING TECHNOLOGIES  

REFERENCES:
10244 VLE32 VLSI TECHNOLOGY

UNIT I CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION 3003
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II LITHOGRAPHY AND RELATIVE PLASMA ETCHING 9
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments,

UNIT III DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALISATION 9

UNIT IV PROCESS SIMULATION AND VLSI PROCESS INTEGRATION 9

UNIT V ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES 9

TOTAL: 45

REFERENCES:

UNIT I
INTRODUCTION TO VLSI TECHNOLOGY
Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array (FPGA)-layout methodologies-Packing-Computational Complexity-Algorithmic Paradigms

UNIT II
PLACEMENT USING TOP-DOWN APPROACH

UNIT III
ROUTING USING TOP DOWN APPROACH

UNIT IV
PERFORMANCE ISSUES IN CIRCUIT LAYOUT

UNIT V
SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION

REFERENCES:
UNIT I
Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion

UNIT II

UNIT III

UNIT IV
Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work test generation procedures.

UNIT V

REFERENCES:
10244AEE41 - ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN

UNIT I  EMI ENVIRONMENT
EMI/EMC concepts and definitions - Sources of EMI - conducted and radiated EMI - Transient EMI - Time domain Vs Frequency domain EMI - Units of measurement parameters - Emission and immunity concepts - ESD.

UNIT II  EMI COUPLING PRINCIPLES
Conducted - Radiated and Transient Coupling - Common Impedance Ground Coupling - Radiated Common Mode and Ground Loop Coupling - Radiated Differential Mode Coupling - Near Field Cable to Cable Coupling - Power Mains and Power Supply coupling.

UNIT III  EMI/EMC STANDARDS AND MEASUREMENTS

UNIT IV  EMI CONTROL TECHNIQUES

UNIT V  EMC DESIGN OF PCBs

TOTAL: 45

TEXT BOOKS:

REFERENCES:
UNIT I

BASIC LEARNING ALGORITHMS
Biological Neuron – Artificial Neural Model - Types of activation functions – Architecture:
Feedforward and Feedback – Learning Process: Error Correction Learning – Memory
Based Learning – Hebbian Learning – Competitive Learning - Boltzman Learning –
Supervised and Unsupervised Learning – Learning Tasks: Pattern Space – Weight
Space – Pattern Association – Pattern Recognition – Function Approximation – Control –
Filtering - Beamforming – Memory – Adaptation - Statistical Learning Theory – Single
Layer Perceptron – Perceptron Learning Algorithm – Perceptron Convergence
Theorem – Least Mean Square Learning Algorithm – Multilayer Perceptron – Back Propagation

UNIT II

RADIAL-BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES:
RADIAL BASIS FUNCTION NETWORKS:
Cover’s Theorem on the Separability of Patterns - Exact Interpolator – Regularization
Theory – Generalized Radial Basis Function Networks - Learning in Radial Basis
Function Networks - Applications: XOR Problem – Image Classification.
Support Vector Machines:
Optimal Hyperplane for Linearly Separable Patterns and Nonseparable Patterns –
Support Vector Machine for Pattern Recognition – XOR Problem - \( \epsilon \)-insensitive Loss
Function – Support Vector Machines for Nonlinear Regression

UNIT III

COMMITTEE MACHINES:
Ensemble Averaging - Boosting – Associative Gaussian Mixture Model – Hierarchical
Mixture of Experts Model(HME) – Model Selection using a Standard Decision Tree – A
Priori and Postpriori Probabilities – Maximum Likelihood Estimation – Learning
Strategies for the HME Model - EM Algorithm – Applications of EM Algorithm to HME
Model
NEURODYNAMICS SYSTEMS:
Dynamical Systems – Attractors and Stability – Non-linear Dynamical Systems-

UNIT IV

ATTRACTOR NEURAL NETWORKS:
Associative Learning – Attractor Neural Network Associative Memory – Linear
Associative Memory – Hopfield Network – Content Addressable Memory – Strange
Attractors and Chaos - Error Performance of Hopfield Networks - Applications of
Hopfield Networks – Simulated Annealing – Boltzmann Machine – Bidirectional
Associative Memory – BAM Stability Analysis – Error Correction in BAMS - Memory
Annihilation of Structured Maps in BAMS – Continuous BAMS – Adaptive BAMS –
Applications

ADAPTIVE RESONANCE THEORY:

UNIT V

SELF ORGANISING MAPS:

PULSED NEURON MODELS:

TOTAL: 45

REFERENCES:
UNIT I    POWER DISSIPATION IN CMOS  
Hierarchy of limits of power - Sources of power consumption - Physics of power dissipation in CMOS FET devices - Basic principle of low power design.

UNIT II    POWER OPTIMIZATION  
Logical level power optimization - Circuit level low power design - Circuit techniques for reducing power consumption in adders and multipliers.

UNIT III   DESIGN OF LOW POWER CMOS CIRCUITS  
Computer Arithmetic techniques for low power systems - Reducing power consumption in memories - Low power clock- Interconnect and layout design - Advanced techniques - Special techniques

UNIT IV    POWER ESTIMATION  
Power estimation techniques - Logic level power estimation - Simulation power analysis - Probabilistic power analysis.

UNIT V    SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER  
Synthesis for low power - Behavioral level transforms - Software design for low power

TOTAL:  45

TEXT BOOKS:

REFERENCES:
UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE 9
Statistical distribution, statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference, safety margin and loading roughness on reliability.

UNIT II RELIABILITY PREDICTION, MODELLING AND DESIGN 9
Statistical design of experiments and analysis of variance, Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis, Petri Nets, State space Analysis, Monte Carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY 9
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV RELIABILITY TESTING AND ANALYSIS 9
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V MANUFACTURE AND RELIABILITY MANAGEMENT 9
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

TOTAL: 45

REFERENCES:
UNIT I MECHANICS OF SPEECH 8

UNIT II TIME DOMAIN METHODS FOR SPEECH PROCESSING 8

UNIT III FREQUENCY DOMAIN METHOD FOR SPEECH PROCESSING 9
Short Time Fourier analysis – Filter bank analysis – Formant extraction – Pitch Extraction – Analysis by Synthesis- Analysis synthesis systems- Phase vocoder— Channel Vocoder.

HOMOMORPHIC SPEECH ANALYSIS:

UNIT IV LINEAR PREDICTIVE ANALYSIS OF SPEECH 10

UNIT V APPLICATION OF SPEECH SIGNAL PROCESSING 10

TOTAL: 45

REFERENCES:
UNIT I  FUNDAMENTALS OF PROGRAMMABLE DSPs  
Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P-DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II  TMS320C5X PROCESSOR
Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

UNIT III  TMS320C3X PROCESSOR
Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design

UNIT IV  ADSP PROCESSORS
Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT V  ADVANCED PROCESSORS

TOTAL: 45

REFERENCES:
2. User guides Texas Instrumentation, Analog Devices, Motorola.
INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS

UNIT I
Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound. Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II
RETIMING, ALGORITHMIC STRENGTH REDUCTION


UNIT III
FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS


UNIT IV
SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES


UNIT V
NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING


TOTAL: 45

REFERENCES: